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Conference Paper

Coder and Decoder of Block 3B4B with Auxiliary Channel

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Abstract

This work presents the coder and decoder of block 3B4B with auxiliary channel. The coder 3B4B converts an input 3 bits word in an output 4 bits word. It transmits an equal number of 1's and 0's to provide a DC constant component. It increases the transitions number, improves the system quality and security. The objective is also to improve the system potentialities with an auxiliary channel to monitor the communication (alarm). The main channel is real, but the auxiliary channel is fictitious.

Keywords: Block codes, Digital systems, Transmission lines

1. Introduction

This work studies the coder and decoder of block 3B4B with auxiliary channel [1, 2, 3, 4, 5, 6, 7, 8, 9, 10]. The auxiliary channel (CA) does not consume physical resources. It is only achieved by programming the appropriate mBnB code in the PROMs (programmable ROM) of the encoder and decoder.

The code must satisfy the rule n=m+1 (m, n integers), to minimize the transmission elevation txo = txi * n/m. Also, n must be even to guarantee a constant DC component with many transitions. Also, m must be low to minimize the system complexity.

The coder converts a three bits word 3B in a word 4B. Posteriorly, the decoder converts newly the four bits word 4B in the original word 3B, recovering the initial sequence.

Fig.1 shows the communication system with relevance for the blocks coder and decoder 3B4B with auxiliary channel.

The coder improves certain characteristics such as:

- Constant DC component what avoids signal fluctuation.

- Sufficient transitions for clock recovery and retiming.
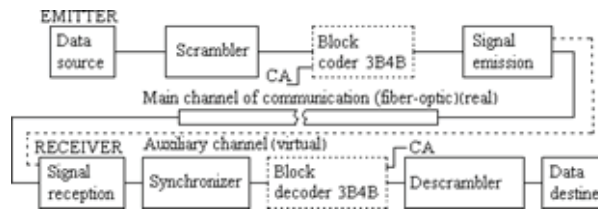
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Figure 1: Communication system with the cod - dec 3B4B auxiliary

- Independent of the bits sequence.

- Decodification independent of the state.

- Multiplication of errors is low.

- Possibility of errors detection.

- Information for alignment of blocks / words.

In emitter, the data source provides the data, the scrambler becomes the spectrum input independent, the line coder equalizes the number of 1's and 0,s, the signal emission adapts the signal to the channel type.

In receiver, the signal receiver provides the electric signal, the synchronizer recoveries the clock, the decoder makes the inverse of the coder, the descrambler makes the inverse of the scrambler and the destination is the final.

The code 3B4B with auxiliary channel is the same normal code 3B4B, where only one word 3B is coded differently, when the CA is zero (CA=0) or one (CA=1).

We choose, for example, the word 3B number 7. Then, it is necessary that two forbidden words belong to the dictionary and codify the situation CA = 1. We choose, for example, the words 1110, 0001 (Tab.1).

TABLE 1: Table of the code 3B4B with auxiliary channel

3B word	+2 Disp.	0 Disp.	-2 Disp.
0- 000	1101		0010
1- 001		0011	
2- 010		0101	
3- 011		0110	
4- 100		1001	
5- 101		1010	
6- 110		1100	
7- 111	1011 '0'		0100 '0'
(7)- 111	1110 '1'		0001 '1'

From a total of 16 words 4B there are 10+2 words for the dictionary (+2D=3, 0D=6, -2D=3). There are 6-2 forbidden words that are [0000, (withdrawal 0001), 0111, 1000, (withdrawal 1110), 1111]. This table produces the followings tables of codification and decodification.

2. Tables of Codification and Decodification

With the code 3B4B auxiliary, we can obtain the table of codification 3B4B and the table of decodification 3B4B.

2.1. Table of codification (PROM - Cod)

A DC constant component implies to send an equal number of 1's and 0's. Then, after to send a positive disparity word, ignoring the 0 disparity word, is necessary to send a negative word and vice-versa (Tab.2).

This table is programmed in the PROM (Programmable Read Only Memory) of the coder.

2.2. Table of decodification (PROM - Decod)

In the decoder PROM must be programmed the corresponding table of decodification (Tab.3)

The words with don't care (11 - - -) are forbidden, can be associated with for example (11 - - -) ≡ (11 010).

3. Pair Coder and Decoder 3B4B

To provide the operation of encoding and decoding tables is necessary to project (create) the hardware of the coder and decoder.

3.1. Coder 3B4B

The codification table is programmed in a PROM, having a flip flop that guards the information of the parity P (positive or negative) of the last transmitted word, according to the status diagram of Fig.2.

<p align="center">TABLE 2: Table of codification 3B4B auxiliary (PROM-Cod)</p>

M + 3B CMA$_2$A$_1$A$_0$	+2 Disp. PB$_3$B$_2$B$_1$B$_0$		0 Disp. PB$_3$B$_2$B$_1$B$_0$	-2 Disp. PB$_3$B$_2$B$_1$B$_0$	
0- 00 000	1 1101				
1- 00 001			0 0011		
2- 00 010			0 0101		
3- 00 011			0 0110		
4- 00 100			0 1001		
5- 00 101			0 1010		
6- 00 110			0 1100		
7- 00 111	1 1011	'0'			
8- 01 000				0 0010	
9- 01 001			1 0011		
10- 01 010			1 0101		
11- 01 011			1 0110		
12- 01 100			1 1001		
13- 01 101			1 1010		
14- 01 110			1 1100		
15- 01 111				0 0100	'0'
16- 10 000	1 1101				
17- 10 001			0 0011		
18- 10 010			0 0101		
19- 10 011			0 0110		
20- 10 100			0 1001		
21- 10 101			0 1010		
22- 10 110			0 1100		
23- 10 111	1 1110	'1'			
24- 11 000				0 0010	
25- 11 001			1 0011		
26- 11 010			1 0101		
27- 11 011			1 0110		
28- 11 100			1 1001		
29- 11 101			1 1010		
30- 11 110			1 1100		
31- 11 111				0 0001	'1'

This states diagram implemented in the flip flop controls the codification mode of the PROM (mode 0 or mode 1).

TABLE 3: Table of decodification 3B4B auxiliary (Prom-Dec)

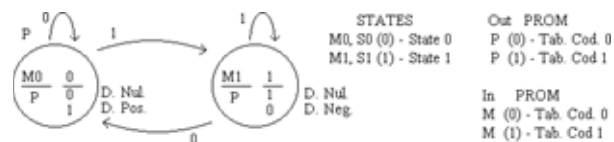| 4B word $B_3B_2B_1B_0$	+2 Disp. $C_1C_0P_1P_0A_2$-A_0	0 Disp., $\notin$D $C_1C_0P_1P_0A_2$-A_0	-2 Disp. $C_1C_0P_1P_0A_2$-A_0
0- 0 000		00 11 - - -	
1- 0 001		Substituted	10 01 111 '1'
2- 0 010			00 01 000
3- 0 011		00 00 001	
4- 0 100			01 01 111 '0'
5- 0 101		00 00 010	
6- 0 110		00 00 011	
7- 0 111		00 11 - - -	
8- 1 000		00 11 - - -	
9- 1 001		00 00 100	
10- 1 010		00 00 101	
11- 1 011	01 10 111'0'		
12- 1 100		00 00 110	
13- 1 101	00 10 000		
14- 1 110	10 10 111'1'	Substituted	
15- 1 111		00 11 - - -	

Figure 2: States diagram of the codification (memory element)

The PROM is the core of the coder. The table, in M=0 is the mode 0 and in M=1 is the mode 1. The table of codification is in the PROM and the states diagram (controller) is in the flip flop memory (Fig.3).
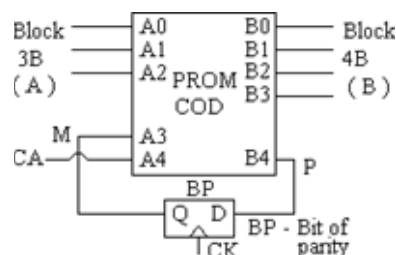

Figure 3: PROM with the codification table 3B4B aux and flip flop

The flip flop receives the disparity P of the anterior word and leads to the correct codification mode (0 or 1). If the disparity P is null, it maintains the codification mode, otherwise it switches to the other codification mode.

In the coder, the data enters in serial 3B, is converted to parallel, coded 3B4B, newly converted to serial 4B and after sent. For this is necessary an input shift register serial - parallel, a normal register, memory PROM and an output parallel- serial shift register. So that this components (architecture) work correctly is necessary a controller based in a clock synthesizer involving two counters of module 3 and 4 and a PLL (Phase Lock Loop) (Fig.4).
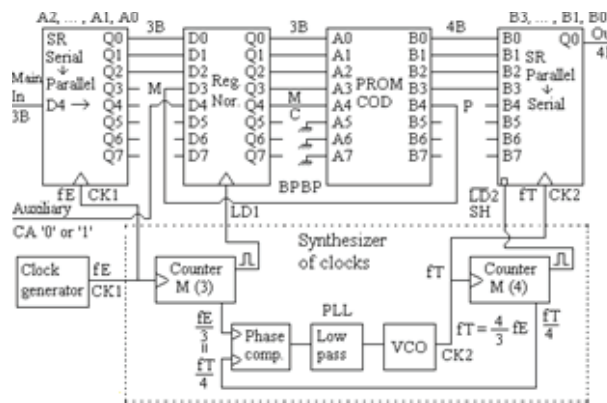

Figure 4: Coder 3B4B

The clock generator is the reference mark (beat) that marks the operation rhythm of the global system.

In the auxiliary channel CA (7, 15, 23, 31), when CA=0 are send the words of NORMAL (1011, 0100), when CA=1 are sent the words of ALARM (1110, 0001).

3.2. Decoder 3B4B

The decodification table 3B4B is programmed in a PROM (Decod), but is necessary that the input words are aligned (marked).

To align correctly the input words 4B is necessary an error detector that detects the forbidden words that don't belong to the codification dictionary and still disrespect the accumulate disparity rule. When occur more than x errors in M, there is suspicion of misalignment and then is activated the alignment mechanism.

The error detector receives information P1P0 of the words forbidden (not belongs to the dictionary) and still the disrespects to the accumulate disparity rule and leads to the error state Se, with output Z = 1 (Fig.5).

The states diagram conduct to the states table, which leads to the circuit of errors detector (Fig.6)
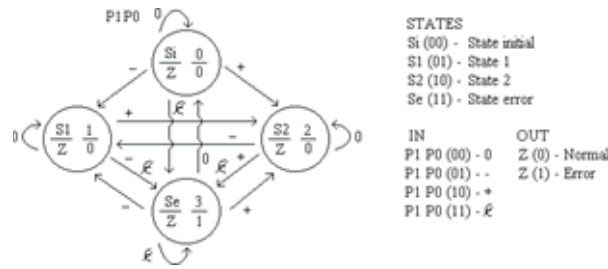
Figure 5: States diagram of the errors detector

Figure 6: States table and respective errors detector

The errors detector was implemented with conventional logic (Karnaugh maps), but could be implemented in a PROM with 2 flip flops (states table) or in a PLD (states diagram).

The PROM (Decod) with the decodification table 3B4B and the errors detector has the configuration of Fig.7.
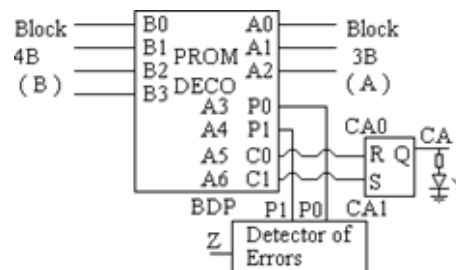

Figure 7: PROM with the decodification table 3B4B and Detector

So that the PROM (Decod) can work (function) correctly are needed various auxiliary circuits. In the decoder, the data enters in serial 4B, it is converted to parallel, decoded 3B4B and after converted newly to serial 3B recovering the original sequence.

For this, is need an input shift register serial - parallel, a normal register, a memory (PROM) and an output parallel - serial shift register. So that this components (architecture) work in perfect harmony is need the controller based in the clocks synthesizer of two counters of

The controller of module 4 can change provisionally the counting module for 4+1=5, in order to make the word alignment, if there is more than $x=8$ word errors in $M=64$ words
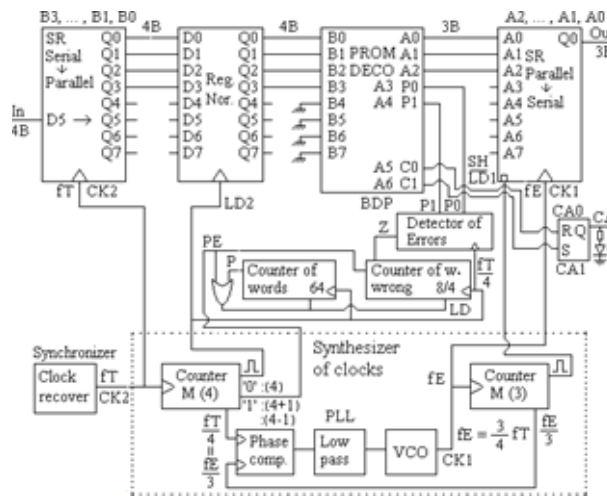
Figure 8: Decoder 3B4B

in the beginning and after 4 word errors in M=64. The clock recover (synchronizer) is the beat that marks the operation rhythm of the entire receiver.

In auxiliary channel CA, when appear the words of NORMAL (1011, 0100), C_1C_0(SR)=01, is made the latch Reset. When appear the words of ALARM (1110, 0001), C_1C_0(SR)=10 is made the latch Set (LED on). For other words C_1C_0=00 and the latch maintains the state.

4. Project, Tests and Results

We present bellow the project, tests and results [5].

4.1. Project

In the pair Coder - Decoder, such as in a digital communication system, is necessary to use good project techniques to create the hardware (architecture) with the able potentiality to execute the desired task. However, is still necessary to make them communicate using a clock synthesizer (controller) that gives unity to the system parts and whose clock is the beater that marks the rhythm.

After designed, the project was tested theoretically in the paper, with a sequence 1' and 0 alternated, however actually the simulation is the tool normally used.

Following, the pair Cod - Decod was mounted and tested in an ebonite bread-board. Finally, with previous performance guaranties, was implemented in printed circuit boards.

4.2. Tests

The pair Cod - Decod was initially connected between itself by a cooper line. In the transitory state, during the power on, occur the inherent errors until to establish the word alignment, which after in the permanent state soon finished and no more appeared.

4.3. Results

The pair Cod-Decod was integrated in the global system with transmission by fibre optic with a gap (air space) that simulated 50 km.

With a degraded signal in its relation signal - noise SNR in the minimum threshold of the CCITT (Comité Consultatif International Teleffonique Telégraphique) / ITU (International Telecomunication Union) the ratio error bits/ total bits BER (Bit Error Rate) of the system (BER - measured) was 10^{-15} and was lesser than the values allowed by the CCITT (BER - CCITT) of 10^{-12}.

This errors 3 - 5 in a period of 24h, have nothing with the pair Cod - Decod, but yes with the fortuitous errors of the synchronizer decision when deciphers '1' or '0' in a signal strongly degraded and indecipherable at human eye.

5. Conclusions

We studied the block coder 3B4B with auxiliary channel.

The coder prepares the data to be transmitted with greater quality and security.

The pair coder decoder 3B4B is based in the code 3B4B programmed in a memory PROM and input serial-parallel and output parallel - serial.

The pair coder decoder needs in the emitter of a clock generator and in the decoder of a synchronizer (clock recovery) that are the reference clock of the synthesizer that controls the work rhythm of all the system.

In the transitory state of start, it arise the inherent alignments errors, that quickly disappear when the permanent state is reached.

With the pair Cod - Decod integrated in the global system, it arise some errors, which are related with the synchronizer decider that is disturbed by the noise.

Anyway, the obtained BER - measured was 10-15 what is lesser than the allowed BER - CCITT that is 10-12.

Acknowledgments

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