

## Conference Paper

# Coder and Decoder of Block mBnB Principally the 1B2B or Manchester

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## Abstract

This work presents the coder and decoder of block mBnB of the type 1B2B or Manchester. In the coder 1B2B each block/word of 1 input bit is coded in the block / word of 2 output bits. In the decoder 1B2B happen the inverse, each block of 2 input bits is newly converted in the original block of 1 output bit. The coder injects in the transmission line a number of 1's exactly equal to the number of 0's, what guarantees a DC constant component and maximizes the transitions number. The objective is to implement the pair coder and decoder 1B2B so that it improves the transmission quality and increases the information security.

**Keywords:** Block codes, Digital systems, Transmission lines

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## 1. Introduction

This work studies the coder and decoder of block mBnB of the type 1B2B or Manchester. It has this name because was created at University of Manchester [1–10].

The coder must satisfy the rule  $n=m+1$ , where  $n$  is integer and even to guarantee an equilibrium between the 1's and 0's. The  $m$  must be integer and near  $n$  to minimize the transmission rate elevation  $t_{xo} = t_{xi} * n/m$ . Also  $n$  must be low in order to minimize the system complexity. The coder injects in the line a number of 1's equal to number of 0's to guaranty a constant DC component and provides transitions to facilitate the clock recovery. The coder 1B2B, in the emitter, converts a block/word of 1 input bit in a block of 2 output bits that is transmitted. The decoder 1B2B, in the receiver, converts the block of 2 bits in the block of 1 bit, recovering the original sequence. Fig.1 shows the communication system with relevance for the blocks coder and decoder 1B2B.

The coder improves certain characteristics such as:

- Constant DC component what avoids signal fluctuation.
- Sufficient transitions for clock recovery and retiming.
- Independent of the bits sequence.

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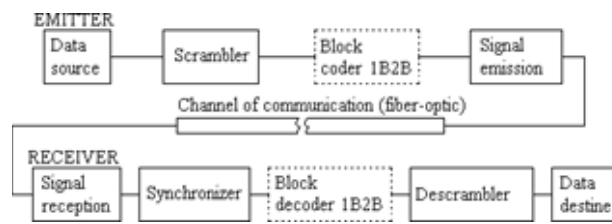


Figure 1: Communication system with the coder - decoder 1B2B

- Decodification independent of the state.
- Multiplication of errors is low.
- Possibility of errors detection.
- Information for alignment of blocks / words.

In the emitter, the data source provides the bits sequence, the scrambler becomes the data spectrum independent of the data source, the line coder codifies the data with equal number of 1's and 0's, the signal emission adapts the signal to the channel. In the receiver, the signal receiver converts the line signal into an electric signal, the synchronizer samples appropriately and retimes the data, the decoder makes the inverse operation of the coder, the descrambler makes the inverse operation of the scrambler and the data destination is the terminal block.

Now, we present the table of code 1B2B (Manchester)

TABLE 1: Code 1B2B or Manchester Data

| NRZ_U D. 1B word | Clock | Operation | Manch. 2B |
|------------------|-------|-----------|-----------|
| 0-               | 0     | XOR       | 01        |
| 1-               | 1     | 0 / 1     | 10        |

From a total of 4 words 2B, 2 words with null disparity (0D) are the dictionary (01, 10). The other two, with disparity 2, are prohibited (00, 11). This table produces the followings tables of codification and decodification.

## 2. Tables of Codification and Decodification

With the code 1B2B, we can obtain the table of codification 1B2B and the table of decodification 1B2B.

## 2.1. Table of codification (PROM - Cod)

To guarantee a constant DC component is necessary to send an equal number of 1's and 0's. In code 1B2B, all the sent words have null disparity. So, the disparity rule is always satisfied. This table don't needs to be desmultiplied as in other block codes (Tab.2).

TABLE 2: Codification 1B2B (PROM - Coder)

| Dec. | 1B $A_0$ | 2B $B_1B_0$ |
|------|----------|-------------|
| 0-   | 0        | 0 1         |
| 1-   | 1        | 1 0         |

This table is programmed in the PROM (Programmable Read Only Memory) of the coder.

## 2.2. Table of decodification (PROM - Decod)

In the decoder PROM must be programmed the corresponding table of decodification (Tab.3)

TABLE 3: Decodification 1B2B (PROM - Decoder)

| D. | 2B $B_1B_0$ |   | 1B $P_0 A_0$ |      |
|----|-------------|---|--------------|------|
| 0- | 0           | 0 | 1            | -(0) |
| 1- | 0           | 1 | 0            | 0    |
| 2- | 1           | 0 | 0            | 1    |
| 3- | 1           | 1 | 1            | -(1) |

This table has the code 1B2B inverted.

The words with don't care (1 -) are forbidden, can be associated with for example (1 - 0, 1 -1).

The disparity violation is not considered, the prohibited words lead immediately to the error state.

## 3. Pair Coder and Decoder 1B2B

To provide the operation of encoding and decoding tables is necessary to project (create) the hardware of the coder and decoder.

### 3.1. Coder 1B2B

The codification table is programmed in a PROM. The sent words have null disparity, then is not necessary a flip flop to guard the parity information P. So, the status diagram is dispensed Fig.2.



Figure 2: States diagram (dispensed)

The modes codification positive/ null and negative/ null are dispensed.

The PROM is the heart of the coder, where is the codification table (Fig. 3).

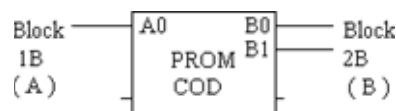


Figure 3: PROM with the codification 1B2B

The sent words have null disparity, so, the coder has only one state.

In the coder, the data enters in serial 1B, is converted to parallel, coded 1B2B, newly converted to serial 2B and after sent. For this is necessary an input shift register serial-parallel, a normal register, a memory PROM and an output parallel-serial shift register. So that this components (architecture) work correctly is necessary a controller based in a clock synthesizer involving two counters of module 1 and 2 and a PLL (Phase Lock Loop) (Fig.4).

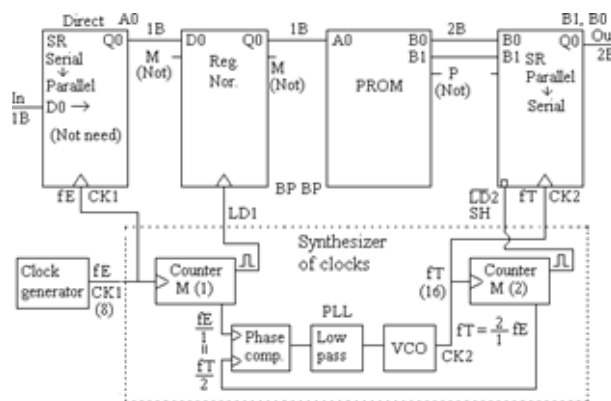


Figure 4: Coder 1B2B

The clock generator is the reference mark (beat) that marks the operation rhythm of the global system.

### 3.2. Decoder 1B2B

The decodification table 1B2B is programmed in a PROM (Decod), but is necessary that the input words are aligned (marked).

To align correctly the input words 2B is necessary an error detector that detects the forbidden words that don't belong to the codification dictionary. The disrespect of the accumulate disparity rule is not applicable. When occur more than x errors in M, there is suspicion of misalignment and then is activated the alignment mechanism.

The error detector receives information P0 of the words forbidden (not belongs to the dictionary) and leads to the error state Se, with output Z = 1 (Fig. 5)

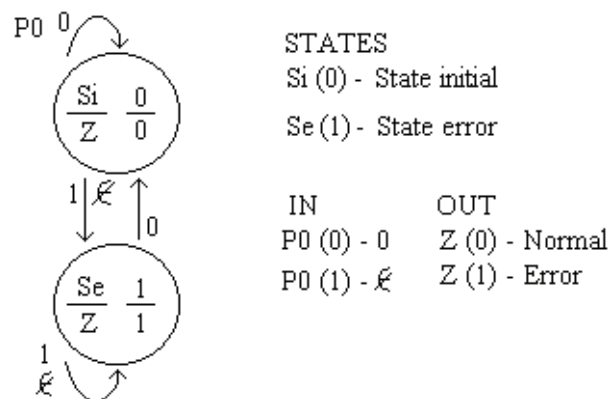


Figure 5: States diagram of the errors detector

The states diagram conduct to the states table, which leads to the circuit of errors detector (Fig.6)

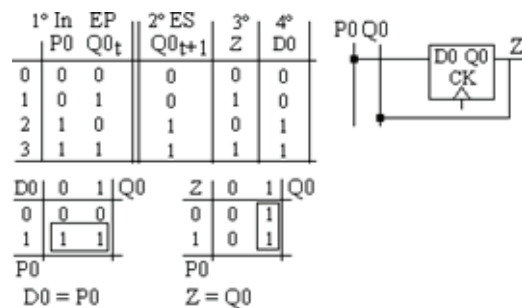


Figure 6: States table and respective errors detector

The errors detector was implemented with conventional logic (Karnaugh maps), but could be implemented in a PROM with 1 flip flop (states table) or in a PLD (states diagram).

The PROM (Decod) with the codification table 1B2B and the errors detector has the configuration of Fig.7.

So that the PROM (Decod) can work (function) correctly are needed various auxiliary circuits. In the decoder, the data enters in serial 2B, it is converted to parallel, decoded

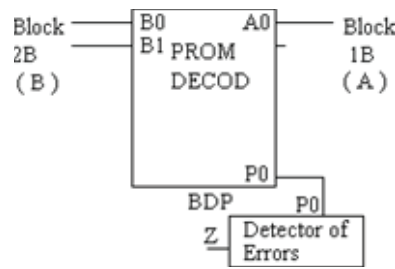


Figure 7: PROM with the decodification table 1B2B and Detector

1B2B inversion and after is converted newly to serial 1B recovering the original sequence. For this is need an input shift register serial - parallel, a normal register, a memory (PROM) and an output parallel - serial shift register. So that this components (architecture) work in perfect harmony is need the controller based in the clocks synthesizer of two counters of module 1 and 2 and a PLL (Fig.8).

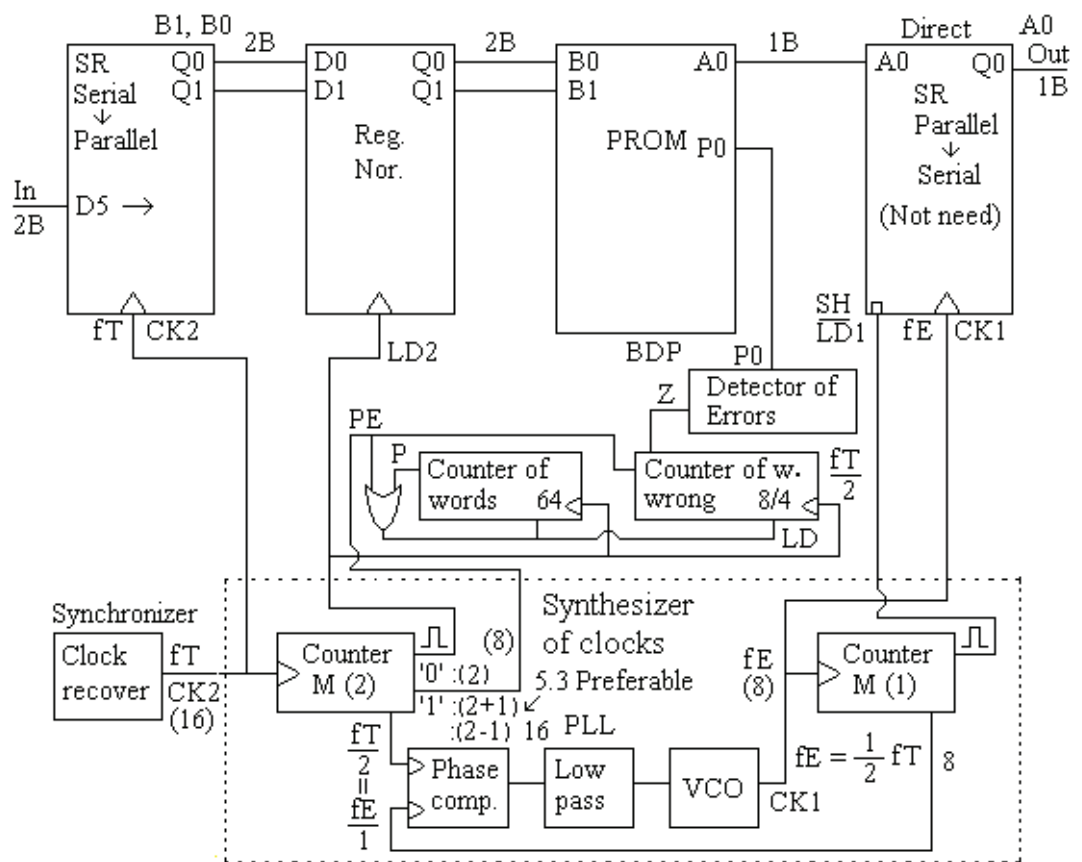


Figure 8: Decoder 1B2B

The controller of module 2 can change provisionally the count module for  $2+1=3$  (preferable) or  $2-1=1$  (not chosen) in order to make the word alignment, if there is more than  $x=8$  word errors in  $M=64$  words in the beginning and after 4 word errors in  $M=64$ .

The clock recover (synchronizer) is the beat that marks the operation rhythm of entire receiver.

## 4. Project, Tests and Results

We present following, the project, tests and results [5].

### 4.1. Project

In the pair Coder - Decoder, such as in a digital communication system, is necessary to use good project techniques to create the hardware (architecture) with the capacity to execute the desired task. However, is still necessary to make them communicate using a clock synthesizer (controller) that gives unity to the system parts and whose clock is the beater that marks the rhythm.

After designed, the project was tested theoretically in the paper, with a sequence '1' and '0' alternated, however actually the simulation is the tool normally used.

Following, the pair Cod - Decod was mounted and tested in an ebonite breadboard.

Finally, with these guaranties, it was implemented in the printed circuit board.

### 4.2. Tests

The pair Cod - Decod was initially connected between itself by a cooper line. In the transitory state, during the power on, occur the inherent errors until to establish the word alignment, which after, in the permanent state finished and no more arose.

### 4.3. Results

The pair Cod-Decod was integrated in the global system with transmission by fiber optic with a gap (air space) that simulated 50 km.

With a degraded relation signal - noise SNR in the minimum limiar of the CCITT (Comité Consultatif International Telephonique Télégraphique) / ITU (International Telecommunication Union) the bit error rate (BER) of the system (BER - measured) was  $10^{-15}$ , which is lesser than the values required by the CCITT (BER - CCITT) of  $10^{-12}$ .

These errors 3 - 5, in a period of 24h, have nothing with the pair Cod - Decod, but yes with the fortuitous errors of the synchronizer decision, when decipherers '1' or '0' in a signal strongly degraded and indecipherable at human eye.

## 5. Conclusions

We studied the block coder mBnB of the type 1B2B. This transmits a number of 1's rigorously equal to the 0's.

The coder prepares the data to be transmitted with greater quality and security. The pair coder decoder 1B2B consist in the code 1B2B programmed in a memory PROM and input serial-parallel and output parallel - serial. The pair coder decoder needs in the emitter of a clock generator and in the decoder of a synchronizer (clock recovery) that are the reference clock of the synthesizer that controls the work rhythm of all the system.

In the transitory state start, the inherent alignments errors arise and quickly disappear when the permanent state is reached.

With the pair Cod - Decod integrated in the global system arise some errors, that are related with the synchronizer decider that is disturbed by the noise.

Anyway, the obtained BER - measured was 10-15 what is lesser than the required BER -CCITT that is 10-12.

## Acknowledgments

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